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SURVEY OF FPGA BASED IMPLEMENTATION OF AREA–DELAY-POWER EFFICIENT RECONFIGURABLE LMS ADAPTIVE FILTER

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Abstract

In digital signal processing LMS filter is used to find out the least mean square error which uses partial product generator. The proposed system uses reconfigurable architecture which is more flexible when compared to the fixed point filter. A strategy is proposed for optimized balanced pipelining across the time consuming combinational blocks of the structure .The objective of the design is to reduce the number of pipelining delays and to reduce the critical path delay. Hence the area, sampling period and energy consumption will be minimized. Lower adaptation delay and low power is achieved by using a novel partial product generator. The proposed design will improve the power delay product (PDP) and energy delay product (EDP) compared to the existing structures.

Keywords: LMS Adaptive filter, Reconfigurable, Power delay product (PDP), Energy delay product (EDP).

I. INTRODUCTION

LMS adaptive filter is the most popular and widely used adaptive filter. In Direct form adaptive filter having a long critical path due to an inner product computing and also produce filter output. To reduce the critical path by using pipelined implementation with exceeds desired sample period.LMS algorithm is not supported pipelining processing. So, it's modified to form Delayed LMS algorithm. To reduce the number of pipeline delay along with the area, sampling period and energy consumption.[1] design is more efficient of the power delay product(PDP) and energy delay product (EDP).we have to use VHDL code and also synthesized by synopsis design compiler using CMOS 65mn library for different filter orders.

It's possible to reduce the power, area and delay more than existing work. The proposed work to use the Re-configurable filter. It produces the better result for us. Re-configurable filter more flexible and also reducing the computational error. The main objective of the design is to reduce the number of pipelining delays and to reduce the critical path delay.

II. EXISTING METHODS FOR REDUCING AREA, POWER AND DELAY BY USING LMS ADAPTIVE FILTER

In [2] Rainy chaplot and Anurag pailwal has estimated the low power and high speed Re-configurable FIR filter based on Novel window technique. Thus authors have combined both window function of Kaiser and Hanning. It over comes the tradeoff between Kaiser and Hanning for power and delay.

Power consumption analysis: We find that the total power consumption (i.e. static and dynamic) increases with increase in order of filter. Power consumption with the proposed window function has an intermediate value then the other two, equal to 67.2 mW (order 10) – 77.2 mW (order 120) for low pass filter and equal to 67.1 mW (order 10) – 76.4 mW (order 120) for high pass filter. Delay analysis: The intermediate delay occurs in the Kaiser-Hanning window function, calculated to be 28.30ns (order 10) – 278.15 ns (order 120) for LPF and 28.30ns (order 10) – 273.06 ns (order 120) for HPF.

In [3] K.Anandan and N.S.Yogaananth have to implement the reconfigurable low power FIR filter architecture. The FIR architecture using Multiplier control decision window (MCSD).This architecture offers 20% power efficient and 40% delay reduction. MSCD architecture achieved high clock frequency compared to direct form architecture. We observed significant area and power reductions over traditional Distributed Arithmetic based techniques and multiplierless technique.
Multiplier control decision window (MCSD): It's used to solve the switch problem. Using control signal generator inside MCSD. The input samples consecutively smaller than threshold are counted and also multiplier is turned off. Vedic multiplier: From normal multiplier for getting better power and speed. In this 16 bit multiplicand A can be decomposed into pair of 8 bits AH-AL. Similarly multiplicand B can be decomposed into BH-BL. The outputs of 8X8 bit multipliers are added accordingly to obtain the 32 bits final product.

In this [4] paper Scott C.Douglar, Quanhong Zhu and Kent F.Smith to design the pipelined LMS Adaptive fir filter architecture without adaptation delay. Fir filter on to parallel and pipelined architecture either introduce delay in the coefficient updates or have excessive hardware requirements. The new architecture throughput is independent of the filter length.
The system output only available after an L-samples delay. Each processing module consists of five multiplication/additions and six register. The algorithm with a variable step size, as this modification does not alter the fundamental form of the algorithm.

In [5] Pramod Kumar Meher and Sang Yoon Park to precise critical-path analysis, we have derived low-complexity architectures for the LMS adaptive filter. Three different structures of direct-form LMS adaptive filter with i) zero adaptation delay, ii) one adaptation delay, and iii) two adaptation delays. Design 2 and Design 3 involve nearly the same (slightly more) EPS than the proposed Design 1 but offer nearly twice or thrice the MUF (Maximum usable frequency) at the cost
Zero adaptation delay: Implementation, both blocks is required to be performed in the same clock cycle. This structure is non-pipelined type. Error computation is performed in the first half cycle. While weight update is performed in the second half cycle.
One adaptation delay: A pipeline latch is introduced after computation of μe_n. There is no register overhead in pipelining. Two Adaptation Delays: Which consists of three pipeline stages, where the first stage ends after the adder tree in the error-computation unit, and the rest of the error-computation block comprises the next pipeline stage. The weight-update block comprises the third pipeline stage.

In [6] Sang Yoon Park and Pramod Kumar Meher, this paper discuss adaptive fir filter based on Distributed Arithmetic (DA).The design increasing the process of parallel lookup table(LUT) updates. The adder based shift accumulation is used inner product computation is replaced by signed carry save accumulation. Fast bit clock using only carry save accumulation unit to reduce the power consumption, but much slower clock is used for other operation.
The design uses two clocks, 1.bit clock, 2. Byte clock. The byte clock is the same as the sampling period. It used in carry save accumulation units and word parallel bit-serial converters. The efficient pipelined architecture for low power, high through put and low area implementation of DA based adaptive filter.

In [7] Lan-Da van and Nu- Siung Feng to design systolic architecture of DLMS adaptive filter. Fir filter design based on a new tree systolic processing element (PE) and also minimized tree level rule .The rule takes minimum delay and high regularity. Systolic fir filter can be easily to identify the maximum driving of the feedback error signal. It is complex to implement DLMS algorithm [13] directly without consideration of systolic techniques. They produce faster convergence, high speed operation and high suitability for VLSI implementation.
The tree structure used for consideration, modularity and local connections. The critical period is independent of other control parameters. The systolic architecture is suitable for single chip realization.

In [8] R.Perry, David R.Bull and A.Nix states to design DFE (Decision feedback equalizer) architecture using DLMS algorithm, and also to compare the convergence and residual mean square error characteristic of the different pipelined filters. The DFE architecture is derived identical processing modules. Order recursive filter (ORF) is used only feed forward section not use feedback filter (FBF), because latency in the output.
The direct form transversal filter (TF), is used pipelined FBF for modified coefficient updating process. Filter structure chosen the FFF's and FBF's to minimize the global communication.

In [9] "Two high performance adaptive filter implementation schemes using distributed arithmetic", Rui Guo and Linda S.De Byunner. The first convention DA, which store sum of weights in LUT's and use addresses to the input. Adaptive filter, necessary to weight updating and must to be update input register. The two type of LUT are used necessary, the auxiliary LUT's are used to update first and then updates of main LUT's are executed.
The second scheme is OBC shown numbers of LUT entries to be reduced without increasing number of LUT's required. No auxiliary LUTs are required for first scheme and also need half memory required for previous work usage exactly. Second scheme only need less than 30% of memory usage for pervious work. The both are also low computational cost.

In [10] C.Preethi and M.Praveena Fixed point LMS adaptive filter with low adaptation delay.LMS adaptive filter contains weight update block with partial product generator (PPG).To produced low adaptation delay and also efficient area, power, delay. The pipelining structure reduces the critical path. The adaptation delay

decomposed two parts. One is fir filtering introduced delay and another part is weight adaptation delay has been involved.
Performance results shows that, the first result shows that LMS adaptive filter with delay. The second output result shows that LMS adaptive filter without delay. The filter achieve without delay given after the clock input. The combinational blocks can be achieved efficient area-delay product and energy delay product.

In [11] Parravi Sathawane and D.V.Prasanthi, this paper to use the low power adaptive filter design for noise reduction. Fir filter designing using two algorithms one is least mean square (LMS) and another one is recursive least squares (RLS) algorithm. Architecture is reconfigurable because dynamically filter order changes with considering amplitude of data sample and filter coefficients. Filter still maintain the performance by the product of data sample and filter coefficient small as the quantization error. The reconfigurable LMS adaptive algorithm is used for reducing the power consumption.

In [12] Asit Kumar Subudhi, Biswajit Mishra and Mihir Narayan Mohantry, this paper deal the LMS algorithm usage of the adaptive filters. In the adaptive filter have to design FIR and IIR model. But the FIR model is more successfully than IIR model in adaptive filters. The LMS algorithm to reduce the computation complexity, good convergence, good stability and also reduce the error at the output of the system.LMS uses a steps size parameter, input signal and the difference of the desired signal and filter output signal to frequently calculate the update of the filter coefficients set. In this algorithm acceptable choice for implement acoustic echo cancellation system, additionally it need for multiplication operation.

III. CONCLUSION

In this paper discussed the LMS algorithm using the adaptive filters, Delayed LMS adaptive filter (DLMS), re-configurable concept, systolic architecture and also application of the adaptive filters. Each technique has a own advantages and drawbacks. All the above techniques mainly focus the low power, area and delay. Future work will be improving the power delay product (PDP) and energy delay product (EDP). That discussion will be very useful for design the LMS adaptive filter and future VLSI circuit designers.

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